Amendments to the Claims

Please amend the claims as follows:

1. (Currently Amended) A timing signal generating circuit which receives a plurality of input signals of differing phases and generates a timing signal having a phase intermediate therebetween, comprising:

a plurality of current polarity switching circuits, each provided between a plurality of current sources and acting to switch an output current polarity in accordance with a corresponding one of said input signals; and

a voltage level correction circuit correcting [[the]] a voltage level of a phase-combined signal produced by combining weighted outputs of said plurality of current polarity switching circuits.

2. (Original) The timing signal generating circuit as claimed in claim 1, wherein said voltage level correction circuit is constructed from a negative feedback circuit.

3. (Original) The timing signal generating circuit as claimed in claim 1, further comprising an amplifying circuit amplifying said phase-combined signal, and wherein said voltage level correction circuit corrects the voltage level of said phase-combined signal to or near an operation point level of said amplifying circuit.

4. (Original) The timing signal generating circuit as claimed in claim 3, wherein said amplifying circuit comprises a plurality of stages of amplifiers in cascade, and said voltage level correction circuit corrects the voltage level for each output of each of said amplifiers.

5. (Original) The timing signal generating circuit as claimed in claim 4, wherein said voltage level correction circuit detects an output voltage average value of said timing signals, and corrects the output voltage average value of said timing signals to or near an operation point level of said amplifier.

6. (Original) The timing signal generating circuit as claimed in claim 3, wherein said amplifying circuit comprises a negative feedback type amplifier.

7. (Original) The timing signal generating circuit as claimed in claim 6, wherein said voltage level correction circuit detects an output voltage average value of said timing signals, and corrects the output voltage average value of said timing signals to or near an operation point level of said amplifier.

8. (Original) The timing signal generating circuit as claimed in claim 1, wherein said timing signal generating circuit generates differential timing signals, and wherein said voltage level correction circuit comprises:

a voltage level monitoring circuit monitoring the voltage level of said differential timing signals; and

a center voltage controlling circuit controlling the center voltage of said differential timing signals based on a reference voltage and an output of said voltage level monitoring circuit.

9. (Original) The timing signal generating circuit as claimed in claim 8, wherein said center voltage controlling circuit directly controls the center voltage of said differential timing signals.

10. (Original) The timing signal generating circuit as claimed in claim 8, wherein said center voltage controlling circuit controls the center voltage of said differential timing signals by adjusting a current in each of said current polarity switching circuits.

11. (Original) The timing signal generating circuit as claimed in claim 10, wherein said center voltage controlling circuit controls the center voltage of said differential timing signals by adjusting a current that flows through a current correction transistor connected in parallel to a current source in each of said current polarity switching circuits.

12. (Original) The timing signal generating circuit as claimed in claim 1, wherein each of said current polarity switching circuits comprises:

a first current source connected to a first power supply line;

a second current source connected to a second power supply line; and

a current polarity switching switch, connected between said first and second current sources, switching current polarity.

13. (Original) The timing signal generating circuit as claimed in claim 12, wherein:

said first power supply line is a high potential power supply line and said second power supply line is a low potential power supply line; and

said first current source is a sourcing type current source which sources a current from said high potential power supply line toward said current polarity switching switch, and said second current source is a sinking type current source which

sinks a current from said current polarity switching switch toward said low potential power supply line.

14. (Currently Amended) A receiver circuit comprising:

a data detection/discrimination circuit detecting and discriminating data carried in an input signal;

a changing point detection/discrimination circuit detecting and discriminating a changing point appearing in said input signal;

a phase comparator circuit receiving outputs from said data detection/discrimination circuit and said changing point detection/discrimination circuit, and comparing the phases of said outputs; and

a clock signal generating circuit receiving an output from said phase comparator circuit, and supplying a first internal clock to said data detection/discrimination circuit and a second internal clock to said changing point detection/discrimination circuit, wherein

said clock signal generating circuit is a timing signal generating circuit which receives a plurality of input signals of differing phases and generates a timing signal having a phase intermediate therebetween, comprising:

a plurality of current polarity switching circuits, each provided between a plurality of current sources and acting to switch an output current polarity in accordance with a corresponding one of said input signals; and

a voltage level correction circuit correcting [[the]] a voltage level of a phase-combined signal produced by combining weighted outputs of said plurality of current polarity switching circuits.

15. (Original) The receiver circuit as claimed in claim 14, wherein said voltage level correction circuit is constructed from a negative feedback circuit.

16. (Original) The receiver circuit as claimed in claim 14, wherein said timing signal generating circuit further comprises an amplifying circuit amplifying said phase-combined signal, and wherein said voltage level correction circuit corrects the voltage level of said phase-combined signal to or near an operation point level of said amplifying circuit.

17. (Original) The receiver circuit as claimed in claim 16, wherein said amplifying circuit comprises a plurality of stages of amplifiers in cascade, and said voltage level correction circuit corrects the voltage level for each output of each of said amplifiers.

18. (Original) The receiver circuit as claimed in claim 17, wherein said voltage level correction circuit detects an output voltage average value of said timing signals, and corrects the output voltage average value of said timing signals to or near an operation point level of said amplifier.

19. (Original) The receiver circuit as claimed in claim 16, wherein said amplifying circuit comprises a negative feedback type amplifier.

20. (Original) The receiver circuit as claimed in claim 19, wherein said voltage level correction circuit detects an output voltage average value of said timing signals,

and corrects the output voltage average value of said timing signals to or near an operation point level of said amplifier.

21. (Original) The receiver circuit as claimed in claim 14, wherein said timing signal generating circuit generates differential timing signals, and wherein said voltage level correction circuit comprises:

a voltage level monitoring circuit monitoring the voltage level of said differential timing signals; and

a center voltage controlling circuit controlling the center voltage of said differential timing signals based on a reference voltage and an output of said voltage level monitoring circuit.

22. (Original) The receiver circuit as claimed in claim 21, wherein said center voltage controlling circuit directly controls the center voltage of said differential timing signals.

23. (Original) The receiver circuit as claimed in claim 21, wherein said center voltage controlling circuit controls the center voltage of said differential timing signals by adjusting a current in each of said current polarity switching circuits.

24. (Original) The receiver circuit as claimed in claim 23, wherein said center voltage controlling circuit controls the center voltage of said differential timing signals by adjusting a current that flows through a current correction transistor connected in parallel to a current source in each of said current polarity switching circuits.

25. (Original) The receiver circuit as claimed in claim 14, wherein each of said current polarity switching circuits comprises:

a first current source connected to a first power supply line;

a second current source connected to a second power supply line; and

a current polarity switching switch, connected between said first and second current sources, switching current polarity.

26. (Original) The receiver circuit as claimed in claim 25, wherein:

said first power supply line is a high potential power supply line and said second power supply line is a low potential power supply line; and

said first current source is a sourcing type current source which sources a current from said high potential power supply line toward said current polarity switching switch, and said second current source is a sinking type current source which sinks a current from said current polarity switching switch toward said low potential power supply line.